## REMARKS

The office is mistaken in refusing to have reviewed identified pending patent applications. It is the undersign's understanding that Applicant is under no duty to supply to the office with *pending* US patent applications. See the Office note at paragraph 30 of the official action–"pending applications" are conspicuously absent in the text of 37 CFR 1.98(a)(2). This requirement is also contrary to the stated goal of being "paperless."

Applicant points out that support for the amendments to the three independent claims above is found as follows:

Independent claim 66: "mass-produced" is found at page 15, line 20. "defect free" is found at page, 31 lines 3-19, page 32 lines 17-19, and page 38, lines 2-10. "40 angstroms" at page 49 line 15. "Atomically smooth". page 44 lines 4-11. "Non-flat" page 37 lines 3-11. "Uniformly" page 6 lines 19-20. Silicon material layer atom-to-atom (page 39, lines 15-17) of silicon substrate must be "intimate". "To avoid excessive leakage current" solving the most critical production problem worldwide disclosed at page 6 lines 8-9.

Independent claim 93 and 95: "Less than 0.5 microns thick" at page line . "Curved ... (bottom) major surface" at page 57, lines 10-12, page 39, line20, and Figs. 4-5. "Mass-produce", "40 angstroms", "atomically smooth", "intimately contacts uniformly" already given in Claim 66 above. "single-material" page 70, lines 14-15. "Gate layer" and "field layer" at page 39, lines 18-20.

Features in the dependent claims not mentioned above are given as follows:

The rejection of claim 87 under 35 U.S.C. §112, second paragraph, is rendered moot. Claim 87 has been canceled.

The rejection of claims 66-67 69-73, 75-82, 85-86, 88 and 93-94 under 35 U.S.C. §103 over US patent No. 6,057,584, Gardner is respectfully traversed.

Those skilled in the art are finding it extremely difficult to form gate layers of less than 15 angstroms. Trial and error is usually invoked in such manufacturing tasks, wherein: for temporary solution of a technical problem, one material is swapped for another, differing process steps are used, or equipment is exchanged without knowing or realizing the problem that has to be overcome in reaching the goal. Thus, thin gate layers holding the promise of low power, high speed and reduced costs remained out of reach over three years after the Gardner patent '584 and world wide one year after Lin's-.US 2002/0164846 publication.

The problem of making an extremely thin gate layer (10 Å) for minimum cost and power but maximum speed still is impossible. An atomic gate or field layer is uniquely critical at least because it is of the ultimate thinness short of going subatomic.

Gardner tries to overcome the problem with a **tri-layer** gate insulating dielectric typified in figs. 2A-2D in which:

layer 1 is a nitrogen-containing oxide layer 204 laid on substrate 202 not for dielectric isolation but to protect the substrate from oxidation (see col. 4, lines 11-14). It has a thickness of from 5 to 10 or more angstroms. By itself this does not overcome the problem. The layer as discussed below is not only defective, but useless when alone.

Layer 2 is an intermediate permittivity oxide layer 206 superposed on layer 202. This layer uses different materials having a dielectric constant ranging from 4 to 100, corresponding to roughly 3 to 5 or 75 to 125 angstrom layer (see Col. 4, line 62 to Col. 5, line 2); and

layer 3 is a high permittivity oxide lay r 208 superpos d on layer 206 and has a thickn ss of from 20 to 50 angstroms (providing a capacitance equivalent to a 3 to 5 Angstrom $SiO_2$ layer ) for a dielectric constant of 40 and a 200 to 500 angstrom layer of a dielectric constant of 400 (see Col. 5, lines 19-41).

All of these layers must work, **in combination**, to make a single useful gate layer. Gardner's gate layers are **flat** and typically formed by chemical vapor deposition, physical vapor deposition, sputtering, jet vapor deposition, rf sputtering, reactive sputtering at for example, 700°C or by thermal oxidation of previously formed Ta metal films (see Col. 5, lines 19-30). There is very little liquid diffusion such as in laser melting, graded seal, metallurgical bonding and **intimately and uniformly** contacting; however there is excess porosity, surface roughness, major defects and "pipelines" (see Col. 5, lines 51-53) which are totally intolerable in modern integrated circuits.

By definition, pipelines are regions of missing atoms of the desired types. Alone, they make it impossible to have an atomically smooth surface. There is also no uniformly intimate contacting of the solid state material layer to the silicon substrate. There is no metallurgical continuity, no graded seal, and no graded chemical composition profiling of the '874 devices.

Further, any semiconductor integrated with such pipelines defects must have high leakage currents unsuitable for any integrated circuit uses. Current gate layers thinner than 15 angstroms all fail because of the high leakage currents.

The methods used by Gardner et al can provide a certain layer thickness but they do not produce an atomically smooth surface. Nor is there **uniformly intimate contact,** local metallurgical continuity, graded seal, and graded chemical composition profiling.

Li in his '175 patent (in column 20, line 43 to column 21,line 5 shows that bonding

of silicon and contacting metals (e.g., tungsten, titanium, cobalt, tantalum, or platinum (Lin et al, publication US 2002/016-4846 A1), silicid s and different oxides (Gardner et al, column 5, lines 8-15) does not provide reliable, reproducible, th rmally and thermochemically stable contacts with graded seal or chemical composition profiling to minimize the thickness and thermal expansion mismatch stresses. This is so regardless of which deposition method is used, such as chemical vapor deposition, physical vapor deposition, jet vapor deposition, RF sputtering ('584 column 5, lines 20-30).

Such deposition methods are always defective, containing, e.g., pipings, voids, and microcracks making the electrical contacting unstable. Yet, the product deteriorates in surface quality, even fractures simply from cooling. Deterioration is primarily due to the extremely high thermal mismatch stresses in the very thin deposited layers. Sputtering, and chemical and physical depositions inevitably yield porous materials and at just 1,000 times magnification show surface roughness. Different grain structures of '584 in column 5, lines 52-53 do not help either, but make it even less possible to have atomically smooth surfaces.

Further, these deposition processes, also used by Lin et al, are basically solid-state particle packing procedures. Even with perfect spheres ideally nucleated according to the closest-packing face-centered cubic or hexagonal structure, the void is about 25%. Since the deposition temperature of 700°C ('584, column 5, lines 23-26) is too low to have liquid filling in the voids for solid density **and liquid smoothing of the surfaces.** Hence, numerous voids and, for very thin films, microcracks must occur to destroy their usefulness as gate or field layers. This is clearly observed by Gardner et al ('594, column 5, lines 50-52).

Page 4, lines 5-17 in '874 states: "The 'heart' of the transistor is the gate dielectric,.... The gate oxide is the smallest but a **critical** feature of the transistor. Shrinking this oxide layer allows more current ... with less voltage. More than any other part of the structure, this layer determines the device performance and reliability." On

page 34, lines 22-23, "the gate layer is the **most critical** part of the MOS or CIS device. Further, serious probl ms still exist." This shows how critical it is to perfect this gate layer and, in particular, to minimize .**the layer thickness**. Unfortunately so far all attempts have failed worldwide." This shows how **critical** is the gate layer and, its thickness.

Further, on page 41, line 19 to page 42, line 1 in '874, material melting and "unidirectional cooling can produce ... columnar grain growth. The anisotropic grains in the bonded regions are highly beneficial to achieve bonds with preferred direction of mechanical **strength** and thermal or electrical **conductivity**. The bonded region then has refined, purified, and burned-in (or aged) gate layer materials with unique and repeatable (superior) mechanical and electrical properties". The **uniformity** results partly because the columnar grain growth is from a liquid melt at ... a liquid diffusion rate of ... about 10 orders of magnitude larger than solid-state diffusion used in Gardner's and Lin's deposition processes.

More importantly, the chemical composition gradient, the thermal mismatch stress gradient are thereby about 5 orders of magnitude smaller. The strength of the silicon-insulator bond between the gate or field layer and the silicon substrate is also about 5 orders of magnitude better with the '874 liquid-diffusion bonding method that with those of Garner's or Lin's methods.

Hence, the liquid-diffusion formed bonds in the '874 devices have **thermal mismatch stress gradients about 5 orders of magnitude smaller** than those in solid-state diffusion formed bonds in Gardner et al and Lin et al. **The strength and *intimacy* of the silicon-insulator ($SiO_2$) bond is therefore also about 5 orders of magnitude stronger in the '874 devices as compared to those of Gardner et al and Lin et al.** Chemical composition or composition profiling, grain sizes, and mechanical properties are also more reproducible.

Without the benefit of melting, there is no surface atomic leveling by atomic surface tension forces, and certainly no atomically liquid-smooth surface (page 50, lines 22-25). The processing temperature of typically 700°C ('584 column 5, line 27) is many hundreds or even thousands of degrees Centigrade too low to melt SiO2, MnO2, TaxOy, barium strontium titanate, and other different oxides ('584, column 5, lines 9-15) to get the atomically smoothed surfaces of the '874 devices. In fact, no commercial deposition equipment appears to be designed to melt these dielectric materials. The rapid heating and splat laser cooling process ('874 at page 59, lines 4-6) would.

Both the top and bottom major surfaces of these layers in the '584 devices are completely flat or planar. There is, therefore, no stress and strain relief from the highly mismatched thermal expansion coefficients (i.e., silicon versus oxide) together with highly mismatched thicknesses (few angstroms vs microns or mils). The result is that these thin film layers must be shattered forming intolerable "pipings", voids, microcracks, leakage paths, unwanted doped lines, ... They would not be useful, at all, for commercial mass-production of high-yield, low-cost devices of the '874 invention.

In addition, the layer 1 of Gardner as above described may be only 5 to 10 angstroms thick, but it is not dielectric insulation. Only layers 2 and 3 are for insulation. The thinner these layers become the greater the defects. Layer 1 must be defective.

Gardner attempted to overcome the "pipping problem" by providing different grain structures. (Col 5, lines 52-53). However, this resulted in additional porosity, reduced strength, less metallurgical continuity, negligible bonding and graded seal. In addition there is less thermochemically stability of the bonding and contacting interfaces among the different thin-film layers and between the thin-film layers and the substrate. Again low device yield due to leakage currents and poor device quality are the result.

The rejection of claims 66, 78, 83-84 and 89-90 under 35 U.S.C. §103 as being unpatentable of US patent publication 2002/0164846 to Lin is respectfully traversed.

The d vices of Lin are actually fabricated from methods deemed better than those used by Gardn r. However; the reference is silent regarding overcoming the problem related to thermal mismatch stresses. There is still no graded seal, and what of the thermochemical stability of the bonding or contacting interface? There are however large defects, voids microcracks and "piping". The thinner layer 14 is the greater are the defects that affect surface roughness. Again Fig, 4 element 14, paragraph 0021 lines 1-7 merely state "preferably in the range of about 50 to 10 Å without providing the artisan direction relative to surface smoothness (see page 31 line 3, to page 34, line 9 and page 39 line 13 to page 39, line 17).

Lin *et al* do not disclose any information as to the 10Å to 50 Å gate layer thickness nor do they provide any detailed information as to how they form their gate layers and, most importantly, they are completely silent about the strength of the boding between the gate layer and the substrate. In addition they fail to detail the thermochemical stability of the contacting interfacial region, and the metallurgical continuity or graded seal. Lin *et al* do not disclose a contacted gate layer material reinforced with solid material-reinforcement. Is the surface of Lin atomically smooth? Lin *et al* fail to provide a useful teaching for making a 10 Å atomically smooth gate layer that is uniformly intimately contacting the substrate. There are no micro photos to show, no operating data presented, and no theories and procedures to overcome the all-critical thermal expansion mismatch problem, particularly when this problem is highly magnified by the greatly mismatched sectional thickness between the layer and substrate.

In sharp contrast, the '874 invention provides:

1) On page 38, lines 2-10, "metallurgical continuity" or uniformity, with "microscopically perfect and continuous, graded bonding ...giving perfect device

structure, continuity, and r p atability";

2) On page 38, lines 8-10, and in claims 66 and 90, "substantially 100% dense, ... defect-free ... with no visible microcracks even at 1,000X magnification";

3) On page 38, lines 12-14,"Bond dissimilar materials ... including oxidized metals and ceramics";

4) On page 38, line 21 to page 39, line 3, and in claims 66, and 67j, 70, and 93-94, "the bond strength can even be more than both ...bonded materials", and material "can be surface-strengthened to be even stronger than the unbonded material itself";

5) On page 39, lines 6-11, the bonded material "can ... selectively withstand 500, 630, 800, and 950 degrees Centigrade ...sufficient for ... any subsequent device processing procedures or service requirements, even for SiC or diamond devices";

6) On page 39, lines 15-17, and in claim 94, "atom-to-atom fusion or liquid diffusion bonds which make the bonds very strong". Silicon atoms contacting air in a void or microcrack in Gardner and Lin's devices certainly have nothing solid to which to bond. There is therefore no atom-to-atom bond at all in all Gardner and Lin's devices;

7) On page 39, line 23 to page 40, line 4, and claims 66, 90, defect-free bonds with no "voids and microcracks [to] give problems of high boron penetration and leakage current, low breakdown voltage, and poor device performance, reproducibility, yield, reliability, and resistance to the ambient particularly as to moisture";

8) On page 40, lines 14-15, and claim 85, solid state material layers with "curvature ... to provide ... stress-relief mechanisms";

9) On page 40, lines 18-20, "Proper bonding of the gate layer ... insures stable

and reliable electrical contacts";

10) On page 41, lines 12–18, and claims 67g, h, j, and j, 70, 75, and 90, "Interface microengineering techniques ... (to) replace failure-initiating oxide or silicon surface voids and microcracks with mechanical, thermal, and electrical strengtheners, material purification and dielectric enhancement, grain refinement and peripheral orientation to facilitate thermal and electrical conduction, and functional composition grading to meet a specific service requirement"; 67, "Interface microengineering techniques ... (to) replace failure-initiating oxide or silicon surface voids and microcracks with mechanical, thermal, and electrical strengtheners, material purification and dielectric enhancement, grain refinement and peripheral orientation to facilitate thermal and electrical conduction, and functional composition grading to meet a specific service requirement";

11) On page 41, line 23 to page 42, line 1, and in claims 67f, and 72, "The bonded region ...have refined, purified, and burned-in (or aged) gate layer materials with unique mechanical and electrical properties";

12) On page 42, lines 5-13, "Chemical composition or composition profiling, grain sizes, and mechanical properties are therefore more reproducible", "dielectric material is purified" to "achieve at least an order of magnitude in material purity";

13) On page 43, lines 2-4, and in claim 95, "Proper melting and freezing is by far the fastest, simplest, and most cost-effective way to produce high-yielding, high-quality semiconductor devices";

14) On page 43, lines 10-15, and in claims 66, 67d and g, 75, 90, "The new gate layer material can be the purest, most defect-free, crystallographically perfect, uniform, with the thinnest but strongest grain or subgrain boundaries, and the exact desired

di l ctric constant. Th subgrains can substantially uniform in width or size and length";

15) On page 45, line 22, to page 46, line 2, and claims 67b, 75, 90, 93, 95-97, the "purified curved gate layer has exception bottom smoothness and minimum microcracks, voids, inclusion, and stresses. As shown, the curvature minimizes mismatch strains and stresses due to thermal expansion, density differences, or volume expansion to form SiO2 from silicon"; while the atomically liquid-smooth surface (page 50, lines 22-25) helps to improve device yield;

16) On page 63, line 22 to page 64, line 1, and claim 85, "In-situ formation of silicon dioxide from silicon via thermal oxidation ... (produces) a volume expansion corresponding to a linear expansion of 29.2%" and an associated compressive stress which is modulated or reduced by a curved gate or junction bottom layer. The residual compressive stress in the gate layer of silicon substrate improves the resistance of the circuit device to tensile fracture. **By definition**, the residual **compressive** stresses in the gate layer of silicon substrate must improve the resistance of the circuit device to, e.g., **tensile** fractures;

Support for additional claim language is found at:

17) On page 78, lines 3-4, "**3-40** angstroms", page 49, line 15, and claims 66 and 95;

18) On page 70, lines 14-15, and claims 67, 88-89, 95, 98, and 100-101 "Single atomic layer ... of ... **insulating silicon oxide or nitride atoms**";

19) On page 69, lines 8-11, and claims 67, 71, 76-78, 80, 83, 89, 95, and 98, "the gate **insulating** layer ... extremely thin, ... one atomic layer ... with about the same accuracy in **lateral dimensions**"; page 78, lines 3-4, "The field layer can be a single atomic layer ... of insulating silicon oxide or nitride atoms 47";

20) On page 45, lines 15-18, and page 57, line 23 to page 58, line 1, and claims 66-67, 78, and 100, "1-2 atomic layers ... of ...$SiO_2$";

21) On page 52, lines 7-10, and claims 66 and 71, "The gate layer ... thin ... flexible ... one to **three atomic layers**";

22) On page 57, lines 4-5, also page 57, lines 13-14; "layer ... only several atoms thick down to a single oxide **molecule**";

23) On page 31, lines 3-4, and claims 66, 70, 93-94, and 100, "gate layer ... perfectly and tenaciously attached to the substrate" for manageable "leakage current (Page 4, line 24), and boron penetration (page 47, line 6) production problems;

24) On page 47, lines 18-22, "The bonding of the gate layer to the substrate generates a wide, liquid-diffusion graded bonding interfacial region ... to reduce the thermal **stress gradient** across the ... region ... (affecting) stress-induced carrier mobilities";

25) On page 48, lines 2-4, and in claim 88 and 98 " Li's '175 metallizing method has "already been successful to join practically all ceramics including: (insulating) **silicon dioxide, silicon nitride**";

26) On page 48, line 9-13, and in claims 66, 67a, c, and g, 83, 90, "not all

the above seven ben ficial qualiti s produced by the ('874) processing method, i. ., atomically surface-smoothed, purified material, extr mely thin gate layer, grain-refinement, flexibility, and perfectly bonded, need all be present on a given device".

27) On page 47, lines 4-6, and claim 66, "providing a perfect gate layer without microcracks which cause unwanted instabilities, leakage currents, and boron penetrations";

28) On page 38, lines 2-10 and 16, and claims 66 and 90, "metallurgical continuity ... microscopically perfect and continuous, graded bonding of ... gate layer to a substrate ... substantially 100% dense, ... defect-free ... with no visible microcracks even at 1,000X magnification" and "extremely high reliability and zero defects";

29) On page 39, line 23 to page 40, line 4, and claim 66, defect-free bonds with no "voids and microcracks ... [have no] problems of high boron penetration and leakage current, low breakdown voltage, and poor device performance, reproducibility, yield, reliability, and resistance to the ambient particularly as to moisture";

30 On page 39, lines 6-11, the bonded **materials are thermochemically stable and** can "... selectively withstand 500, 630, 800, and 950°C ...sufficient for ... any subsequent device processing procedures or service requirements, even for SiC or diamond devices";

31) On page 40, lines 18-20, "proper bonding of the gate layer ... insures

stable and reliable lectrical contacts".;

32) On page 44, lines 4-11, and claims 67a, and c, 83, and 90, "smooth .... by an atomic surface-smoothing mechanism, i.e., atomic surface tension forces ... achieving minimum roughness";

33) On page 50, lines 19-24, and claims 66-67, 83, 90, and 93-94, "gate layer (via) atomic surface-smoothing process to achieve a liquid-smooth surface ... has atomic surface forces ... to produce the liquid-planar ... surface" helping to improve device yield;

34) On page 45, line 22 to page 46, line 2, and claims 66-67, 83, 75, 90, and 93-94, "purified curved gate layer has exceptional bottom smoothness and minimum microcracks, voids, inclusion, and stresses. ... the curvature minimizes mismatch strains and stresses due to thermal expansion, density differences, or volume expansion to form $SiO_2$ from silicon";

35) on page 57, lines 10-12 and page 56, line 9, and claims 66, 68-69, 85-86, 94, 96, and 101, "oxide isolating grooves (with) **zero bottom width** avoiding **flat portions** on prior-art devices";

36) On page 50, line 1, and claims 67, 85-86, 88, and 91-97, "gate layer ... a concave curved surface";

37) On page 16, line 22, "gate or field layer", and claims 80, 92, 95, and 97;

38) On page 51, line 24 to page 52, line 6, and claim 74, "curved depression (or gate layer) designed to reduce ...thermal mismatch stresses through a curvature-related stress-relief mechanism ... Gate layer ... have a concave shape when looked from ... above ... with a radius of curvature of less than 0.5 microns" (or 1 micron on page 58, lines 5-7);

39) On page 41, line 19 to page 42, line 7, and claims 66-67, and 93-94, "Unidirectional cooling can produce ... columnar grain growth. The anisotropic grains ... are high beneficial ... with preferred direction of mechanical strength and thermal or electrical conductivity. The bonded regions ... have refined, purified, and burned-in (or aged, page 51, lines 20-21) gate layer material with ... **repeatable** mechanical and electrical properties. The **uniformity** results ... from a liquid melt ... (with) liquid diffusion rate ...about 10 orders of magnitude larger than solid-state diffusion rates (in Gardner and Lin's deposition processes) ...Chemical composition or composition profiling, grain sizes, and mechanical properties are therefore more reproducible";

40) On page 43, lines 10-14, and claim, 66 and 67, "the new gate layer ... can be the purest, most defect-free, crystallographically perfect, uniform, with the thinnest but strongest grain or subgrain boundaries, and the desired dielectric constant".

41) On page 22, lines 10-12, "size (e..g, length, width, and depth) of implanted region ... less than ... 10 angstroms";

42) On page 70, lines 4-13, and claims 69, 77, and 98, "implanting ...

oxygen and nitrogen ...to a few atomic layers", (ion) "implanted layer ... l ss than ... a few atomic layers... sizes ... accurate ... to several angstroms in depth, lateral dimensions, ... and chemical composition profiles";

43) On page 41, lines 22-23, "bonded regions ... burned-in" or aged, supporting claims 67g nd 72;

44) On page 51, lines 10-12, and claim 67, 90 "most material purification occurs precisely at the lower or first-to-freeze layer closest to the substrate";

45) On page 40, line 21-23, "Layer ... by proper metallizing," and "Metallized ceramics according to Li's '175 patent helps to achieve perfect bond";

46) On page 42, lines 5-13, and claim 75, "Chemical composition or composition profiling, grain sizes, and mechanical properties are therefore more reproducible", "dielectric material is purified" to "achieve at least an order of magnitude in material purity";

47) On page 52, lines 15-18, and claim 84, "gate layer has ... less than about 10 ppm of impurities"; and Page 52, line 20 to page 53, line 2, "Because of the ... same composition, the gate layer, the substrate, the pockets, and even the gate lead all have substantially ...density, minimizing dynamic stresses due to vibrations, impacts, and high accelerations and decelerations";

48) On page 70, lines 14-15, and claims 67,72,80,84,88-89,amd 95-96, "Single atom layer ... of insulating silicon oxide or nitride;

49) On page 9, lin s 2-3, and claim 99, "very shallow ... junction (region d pth)" of no more than "70 nanometers"; and

50) Figures 4 and 5 supports claims 66, 68, 78-79, 83-86, 89, and 93-95.

The following features are not new by themselves. But they should be allowed in view of their dependent claims.

51). On page 3, lines 17-19 support the lists of substrate materials support claim 81; while page 3, line 23 to page 4, line 5 support useful solid state devices support claim 82; and

52) On page 40, lines 23 to page 41, line 3, "a conductive gate electrode formed of an electrically conducting material is generally centered on the gate area to control flow of electronic carriers from ... source to the drain" supports claim 89.

It is submitted neither the Gardner et al patent nor the Lin et al patent produces circuit devices have any of the above patentable features 1 through 50.

As shown above, both these cited references use vapor deposition methods to form the gate layer, at a typical temperature of about 700°C ('584, column 5, lines 24-26). This temperature is hundreds or even thousands degrees lower than the melting point of either silicon, silicon oxide, silicon nitride, and the like. These deposition processes involve no melting, no liquid diffusion, no atomic surface smoothing by surface tension, no filling of surface "pipings", voids, and microcracks to achieve surface strengthening, and many of the above 16 features.

Yet, this same deposition temperature is already 3.5 times the allowable temperature without fracturing the silicon dioxide. On page 62, lines 7-25 specially lines 24-25, "Hence, a circuit processing step involving a temperature change of mere 199 degrees Centigrade can fail the thin, straight (or flat) oxide layer." It is, therefore, no wonder that Gardner et al see oxide failures in the form of "pipings", a special type of voids and microcracks in their circuits.

In view of the above, applicant respectfully submits that the rejections are made in error and should be withdrawn.

In view of the amendments and remarks above, Applicants submit that this application is in condition for allowance and request reconsideration and favorable action thereon.

Any fee not covered and required for entry of this amendment should be charged to the undersign's deposit account 50-1770.

Respectfully submitted,

James A. Poulos, III
Attorney for applicant
Reg. No. 31,714

FAX RECEIVED
AUG 11 2003
TECHNOLOGY CENTER 2800

OFFICIAL

Atty. Docket No. Ii,

9001 Garland Ave
Silver Spring, MD 20901
Tel: (301) 495-6341
Fax: (301) 495-6341

The Undersigned certifies that this amendment was filed by facsimile on August 11, 2003, to 703 ~~302 7722~~ 872-5318 along with a petition for extending the response two months.

James A. Poulos, III

August 11, 2003